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cont.

1 2. (amended) The driver circuit as claimed in claim 1, wherein the at least one input
2 node for the input signal is connected to the at least one sub-driver.

1 3. (amended) The driver circuit as claimed in claim 2, wherein the at least one input
2 node for the input signal is connected to the at least one evaluation circuit.

1 4. (amended) The driver circuit as claimed in claim 1, wherein two or more sub-drivers
2 and two or more evaluation circuits are provided, each sub-driver being connected to an
3 evaluation circuit.

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1 5. (amended) The driver circuit as claimed in claim 4, wherein two or more feedback
2 capacitors are provided, each feedback capacitor being provided between an output node of the
3 driver circuit and an input node of an evaluation circuit.

1 6. (amended) The driver circuit as claimed in claim 1, wherein the input node(s) of
2 the evaluation circuit(s) is/are at low impedance.

1 7. (amended) The driver circuit as claimed in claim 1, wherein the at least one sub-
2 driver has one or more transistors.

1 8. (amended) The driver circuit as claimed in claim 1, wherein at least one control
2 transistor is provided in the at least one sub-driver, said transistor being respectively connected
3 to an evaluation circuit.

1 9. (amended) The driver circuit as claimed in claim 1, wherein the at least one
2 feedback capacitor is designed as a linear capacitor.

1 10. (amended) The driver circuit as claimed in claim 1, wherein the at least one
2 feedback capacitor is designed as a nonlinear capacitor.

1 11. (amended) The driver circuit as claimed in claim 10, wherein the nonlinear
2 capacitor is formed from at least one PMOS transistor and/or at least one NMOS transistor.

1 12. (amended) A method for operating a driver circuit as claimed in claim 1, wherein
2 a low-harmonics current is generated in the driver circuit and supplied to a load, and wherein an
3 edge steepness that is independent of the present load situation is set in the driver circuit.

1 14. (amended) The method as claimed in 12 wherein, in order to set the load-
2 independent edge steepness, the output characteristic of the driver circuit is measured by the
3 feedback circuit and evaluated therein, and wherein the drive strength of the at least one sub-
4 driver is regulated on the basis of the evaluation results.

1 16. (amended) The use of a driver circuit as claimed in claim 1 of a method as
2 claimed in claim 12 for improving the electromagnetic compatibility of electronic components,
3 in particular of integrated circuits.

In the Claims

1 1. (amended) A driver circuit, having at least one input node [(11)] for an input
2 signal and at least one output node [(12)] for an output signal, having one or more, preferably
3 two, sub-drivers [(20, 30)] and having a feedback circuit [(40)], which has one or more
4 evaluation circuits [(50, 60)] and one or more feedback capacitors [(41, 42)], the evaluation
5 circuit(s) [(50, 60)] being connected to the sub-driver(s) [(20, 30)] and the feedback capacitor(s)
6 [(41, 42)] respectively being provided between an output node [(12)] of the driver circuit [(10)]
7 and an input node [(51, 61)] of an evaluation circuit [(50, 60)], the at least one evaluation circuit
8 [(50, 60)] having a first inverter stage [(53, 54)], coupled to the input node [(51, 61)] of the
9 evaluation circuit [(50, 60)], and also a second inverter stage [(56, 57)], connected in series with
10 the first inverter stage [(53, 54)], the first inverter stage [(53, 54)] being short-circuited with the
11 input node [(51, 61)].

1 2. (amended) The driver circuit as claimed in claim 1, wherein the at least one input
2 node [(11)] for the input signal is connected to the at least one sub-driver [(20, 30)].

1 3. (amended) The driver circuit as claimed in claim [1 or] 2, wherein the at least one
2 input node [(11)] for the input signal is connected to the at least one evaluation circuit [(50, 60)].

1 4. (amended) The driver circuit as claimed in [one of] claim[s] 1 [to 3], wherein two or
2 more sub-drivers [(20, 30)] and two or more evaluation circuits [(50, 60)] are provided, each sub-
3 driver [(20, 30)] being connected to an evaluation circuit [(50, 60)].

1 5. (amended) The driver circuit as claimed in claim 4, wherein two or more feedback
2 capacitors [(41, 42)] are provided, each feedback capacitor [(41, 42)] being provided between an
3 output node [(12)] of the driver circuit [(10)] and an input node [(51, 61)] of an evaluation circuit
4 [(50, 60)].

1 6. (amended) The driver circuit as claimed in [one of] claim[s] 1 [to 5], wherein the
2 input node(s) [(51, 61)] of the evaluation circuit(s) [(50, 60)] is/are at low impedance.

1 7. (amended) The driver circuit as claimed in [one of] claim[s] 1 [to 6], wherein the
2 at least one sub-driver [(20; 30)] has one or more transistors [(21, 22, 23; 31, 32, 33)].

1 8. (amended) The driver circuit as claimed in [one of] claim[s] 1 [to 7], wherein at
2 least one control transistor [(24, 34)] is provided in the at least one sub-driver [(20, 30)], said
3 transistor being respectively connected to an evaluation circuit [(50; 60)].

1 9. (amended) The driver circuit as claimed in [one of] claim[s] 1 [to 8], wherein the
2 at least one feedback capacitor [(41, 42)] is designed as a linear capacitor.

1 10. (amended) The driver circuit as claimed in [one of] claim[s] 1 [to 9], wherein the
2 at least one feedback capacitor [(41, 42)] is designed as a nonlinear capacitor.

1 11. (amended) The driver circuit as claimed in claim 10, wherein the nonlinear
2 capacitor is formed from at least one PMOS transistor [(43)] and/or at least one NMOS transistor
3 [(44)].

1 12. (amended) A method for operating a driver circuit as claimed in [one of] claim[s]
2 1 [to 11], wherein a low-harmonics current is generated in the driver circuit and supplied to a
3 load, and wherein an edge steepness that is independent of the present load situation is set in the
4 driver circuit.

1 14. (amended) The method as claimed in 12 [or 13,] wherein, in order to set the load-
2 independent edge steepness, the output characteristic of the driver circuit is measured by the
3 feedback circuit and evaluated therein, and wherein the drive strength of the at least one sub-
4 driver is regulated on the basis of the evaluation results.

1 16. (amended) The use of a driver circuit as claimed in [one of] claim[s] 1 [to 11
2 and/or] of a method as claimed in [one of] claim[s] 12 [to 15] for improving the electromagnetic
3 compatibility of electronic components, in particular of integrated circuits.